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FIRST QUARTERLY REPORT

21 June 1963 to 30 September 1963

BROADBAND MICROWAVE POWER LIMITERS

Contract NObsr-89462

Project Serial No. SR-0080302

Task 9637

Navy Department, Bureau of Ships

MICROWAVE ASSOCIATES, INC.
BURLINGTON, MASSACHUSETTS

MICROWAVE ASSOCIATES, INC.

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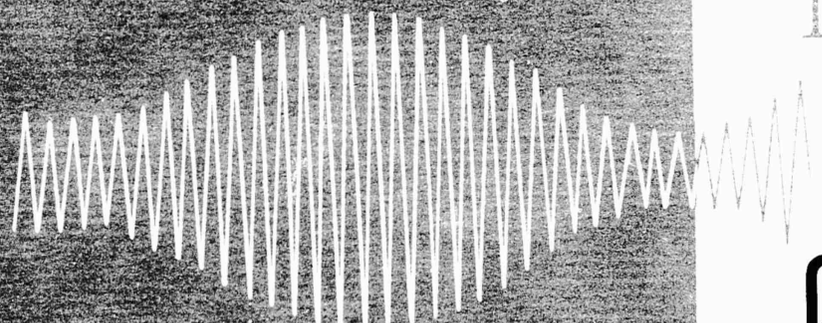

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MICROWAVE ASSOCIATES, INC.

BURLINGTON, MASSACHUSETTS

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ABSTRACT

This report contains results secured during the initial study phase of this contract. Sections are devoted to discussion of the basic diode limiter concept, limiter diode characteristics and diode packaging considerations.

Also included is a quantitative treatment of the "ideal" diode limiter circuit and its limitations with respect to the direct problems of concern.

Concluding the technical study presented in this report is a discussion on broadband diode limiter designs capable of achieving multi octave bandwidths below 5 Kmc and octave bandwidths between the range of 5 Kmc to 11 Kmc.

PART I

PURPOSE

The purpose of this contract is to develop a family of broadband high power limiters covering the range of 1 Kmc to 11 Kmc. Proposed design goal specifications for these limiters are listed as follows:

	(a)	(b)	(c)
Frequency Range, Kmc	1-4.5	4-7.5	7-11
Maximum Operating Peak Power, KW	10	5	1
Maximum Average Power, W	10	5	1
Maximum Pulse Width, μsec	10	1	1
Maximum Spike Leakage, Ergs	0.5	0.5	0.3
Maximum Flat Leakage, Watts	0.040	0.040	0.040
Maximum Insertion Loss, DB	0.5	1.0	1.0
Transmission Line Form	Coax	Coax	W/G

GENERAL FACTUAL DATA

1. THE DIODE LIMITER CONCEPT

The microwave diode limiter can be basically stated as being a power sensitive passive attenuator based on the nonlinear properties of microwave PN-junction* diodes. When low power levels are incident upon the limiter structure (less than 1 mW), and within the rated operational frequency range, negligible loss will be encountered. Therefore, the limiter will act as a section of matched transmission line with some small finite loss. In the case of a high power level incident upon the limiter structure, a high degree of loss takes place and the limiter will act as a highly mismatched section of transmission line. With respect to the power lost in this case, it will be due to both reflection and dissipation with the former being greatly dominant due to power capability considerations. Obviously, this consideration is of extreme importance since the power dissipated by the limiting diode or diodes will primarily determine maximum power handling capability of the limiter.

In addition to the power sensitivity operational characteristics of the limiter, one other important characteristic is displayed. This is the fact that the limiter is completely passive in operation with respect to prior knowledge of input signal characteristics. That is, no information need be supplied from the systems that the limiter is

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*Point contact diodes will not be considered due to their inherent low power handling capability.

employed in or used to protect against.

In general, the PN-junction diode limiter can be considered as being a solid-state equivalent of the conventional gaseous TR-tube. However, in theory it does not suffer from the TR-tube drawbacks such as life and inter-pulse protection. While it seems unlikely that PN-junction diode limiters will replace TR-tubes on the basis of power handling capability, its octave bandwidth capability of operation offers a feature previously unobtainable.

2. SEMICONDUCTOR LIMITER DIODES

In the area of control of microwave power through use of semiconductors, two main PN-junction type diodes have become prominent. These are the varactor and PIN diode. In Figure (1), general characteristics of both types are compared on the basis of construction, equivalent circuit and impedance characteristics at microwave frequencies. As can be seen, the varactor can be characterized as a voltage dependent capacitance while the PIN diode exhibits all essential properties of a voltage dependent resistance.

In addition to the properties shown in Figure (1), both diode types exhibit the normal current voltage relationship of the classic PN-junction. This takes the form of a sharp current rise when subjected to a small forward bias (+ on the P side) and an avalanche breakdown condition with the application of some comparatively large reverse bias.

Because each diode can exhibit a radical change of impedance state at microwave frequencies, their application to passive control of microwave power can at once be appreciated. This is well illustrated by the Smith Chart impedance plots shown in Figure (1). However, one other necessary property must first be investigated and this is the ability of the diode to interact directly with an applied RF waveform at microwave frequencies. Basically, this amounts to rectification efficiency and charge storage characteristics of the diode in the frequency range of concern.

(2-a) THE VARACTOR DIODE

In Figure (1), the varactor constructional schematic shows it to consist of a $P^{+}NN^{+}$ sandwich arrangement of semiconductor material, thereby creating a PN-junction. At zero bias, it is at equilibrium as a result of holes and electrons distributing themselves such that there are essentially no carriers in the vicinity of the junction. This region which is free of electrons and holes is called the depletion layer. Its presence enables the varactor to exhibit the required characteristic of a parallel plate capacitor with the depletion layer forming the separation between two conductive regions. In order to control magnitude of capacitance, junction area can be varied in size. Here again, the effects are identical to that obtained with variation of area in a parallel plate capacitor.

If a potential were now applied across the semiconductor junction, the depletion layer would change in thickness due to charge movement and therefore vary capacitance. If made sufficiently large and positive in

polarity, the normal forward conduction process of a PN-junction would occur. In regard to varactors, no difficulty has been encountered with respect to this process responding faithfully to an applied RF voltage of relatively low power level (0.1 - 0.5 watts). This can be attributed to the fact that holes and electrons need only move a small portion of the depletion layer width.[1] At higher power levels, a considerable amount of carriers, both holes and electrons, are injected into the N region with an effective disappearance of the depletion layer. In fact, this occurs to such a degree that the negative RF voltage excursions are unable to sweep out an appreciable portion of this charge. The varactor will then appear as having an infinite capacitance and hence very low impedance.

The varactor equivalent circuit, as shown in Figure (1), contains a series resistance R_s in addition to its voltage dependent capacitance. This primarily arises from resistance associated with the base region and is constant until appreciable forward conduction takes place. When this occurs, the injection of carriers as described in the previous paragraph can cause a large reduction in series resistance* by as much as 80%. This process is termed conductivity modulation and is illustrated in the varactor impedance plot of Figure (1) by deviation from the

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[1] Uhlir, A. Jr. "The Potential of Semiconductor Diodes in High Frequency Communications." Proc. IRE, Vol. 46 pp 1099-1115 (June 1958).

* This effect is normally very pronounced in silicon varactors and may or may not be evident in other semiconductor material types.

constant resistance circle. In this case, it is caused by a DC voltage but will also occur under RF conditions to a lesser degree. The new value of resistance will be referred to as $\bar{R}_s$ whether caused by a DC or RF voltage applied across the PN-junction.

(2-b) THE PIN DIODE

The PIN diode[2], though similar to the varactor, contains one important constructional difference. This is the inclusion of a relatively thick intrinsic semiconductor region (I region) between P^+ and N^+ material layers. Because of this, the PIN diode exhibits a much larger area per unit capacitance and higher avalanche breakdown rating as compared to varactors. The variable resistance property of the PIN diode is caused by injection of both holes and electrons into the I region upon the application of a forward bias. This creates an effective electron-hole plasma in what was formerly a dielectric region, thus converting it into a conducting medium. The overall result is that the PIN diode is changed from a very high to a very low resistance as illustrated by its typical Smith Chart impedance plot in Figure (1). Also illustrated in this plot is the effect of C_p in the region from zero to reverse breakdown. This tends to make the PIN diode appearance deviate slightly from a pure variable resistance.

With respect to the PIN diode interacting directly with an applied RF voltage, serious difficulties can be encountered. This

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[2] Leenov, D. Forster, J. H., Crann, N. "PIN Diodes for Protective Limiter Applications." Solid-State Circuits Conference Digest, pp. 84-85, 1961.

occurs by virtue of the requirement that an appreciable distance must be travelled by carriers in order to create an effective low resistivity electron hole plasma. For typical PIN diodes, this effect is quite pronounced at L-band. It can be considered a form of transit time phenomenon since reduction in I region thickness will improve the situation. However, the ultimate of this approach is degeneration into the basic varactor design with its relatively high capacitance per unit area characteristic. Thus, larger power handling capabilities of the PIN diode by virtue of comparative junction size is lost.

Therefore, as can be seen, the PIN diode does not directly lend itself to high power limiting applications due to its relatively slow interaction time with an applied RF waveform. This inability precludes its use as a microwave power limiter in the normal sense of operation but has little effect on its ability to be used as a moderately fast switch driven by an external bias source. However, as was previously stated, only passive devices are of concern here so that synchronized driving pulses cannot be supplied from an external source.

By utilizing a hybrid form of operation which combines aspects from both diode limiting and switching concepts, a truly passive PIN limiter capable of operating at higher microwave frequencies can be achieved. The circuit required to achieve this is shown in Figure (2). As shown, the PIN diode is placed in shunt across a transmission line in a suitable microwave switching circuitry configuration*. Preceding

*Details of appropriate diode circuitry will be described in section 4 of this report.

the PIN diode is a signal sampling device (directional coupler) terminated by a high burnout xtal diode. This diode is of the point contact type and has an exceedingly fast response time.

As an incident RF signal is applied, a portion will be delivered to the xtal diode. Its rectified video output is then fed to the PIN diode, causing it to change to a forward conduction state and become highly reflective. This constitutes an effective limiter action whose threshold of limiting is controlled by the xtal diode decoupling magnitude with respect to the main transmission line.

Attractive as this approach may seem, it still has several drawbacks. The most important is due to the fact that a leakage spike in the RF waveform will be present due to the relatively long switching time required by the PIN diode. However, this can be compensated for by following the PIN limiter by a conventional varactor type which will in effect greatly reduce the spike amplitude. The other drawback concerns recovery time. Here again, slowness of response of the PIN diode is evident because a finite time is required for it to change from a conducting to non-conducting state. This makes it self evident in the form of a finite recovery time*. However, here several schemes, which will be covered in later reports, exist which enable recovery time values much less than a μsec to be obtained.

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*The conventional 3 DB point for recovery time is assumed here as in the case of TR-tubes.

Despite the above mentioned disadvantages, the PIN diode in a feedback limiter configuration can be advantageously employed where initial reduction of high power levels is of concern. Once accomplished, conventional varactor limiters can be used to cope with the remaining power levels. Therefore, the PIN feedback limiter can be considered as a solid-state equivalent of the normal gaseous pre TR-tube.

3. DIODE PACKAGE CHARACTERISTICS

Before proceeding into a discussion on PN-junction diode limiter circuitry, a more detailed knowledge must be gained with respect to the actual diode equivalent circuit. At very low frequencies, the equivalent diode circuit can be considered as that of the PN-junction alone. However, in the frequency range of concern, 1 Kmc to 11 Kmc, the effect of physically packaging the diode must be considered.

Unfortunately, once the diode is packaged, stray reactances are introduced that must be accounted for in the microwave circuitry environment. These take the form of inductance, L_s, in series with the diode junction and a shunt capacitance, C_p, in parallel with the previous combination. The general diode package equivalent circuit is shown in Figure (3). Also shown is a series equivalent representation that lends itself more easily to circuit performance calculations that will be discussed later. The necessary transformation equations for the series representation are listed below.

$$R_T = \frac{X_p^2 R_s}{R_s^2 + (X_s + X_p)^2} \tag{1}$$

$$X_T = \frac{X_p R_s^2 + (X_s + X_p) X_s X_p}{R_s^2 + (X_s + X_p)} \tag{2}$$

where $X_p = -\frac{1}{\omega C_p}$

$$X_s = \omega L_s - \frac{1}{\omega C_s}$$

L_s is the parasitic series inductance

C_p is the parasitic shunt capacitance

R_s is the diode junction series resistance

C_s is the diode junction series capacitance

In the case where either a forward current bias or high power is employed, a bar notation will be used. Therefore, R_s will become $\bar{R}_s$ and X_s changes to $\bar{X}_s$. As for the latter, it can be assumed to be ωL_s under forward bias since C_s will approach infinity. With respect to C_p and L_s, they are fixed and therefore unaffected by bias conditions.

(3-a) CERAMIC PACKAGE DIODES

In Figure (4), various typical diode package types are shown which will be employed in future circuit development on this contract. They are of ceramic package construction with the ceramic portions indicated. The pill type, shown in Figure (4-a), has been manufactured by Microwave Associates for the past several years and

results to date show it to be extremely rugged in nature. Though shown with two connecting prongs, threaded studs can be substituted if desired or one stud removed completely.

The μ-stick package design, shown in Figure (4-b), is of a recent design and is still undergoing development. However, prototype units have been fabricated and tests to date show a large improvement with respect to parasitic reactance as shown in the table of Figure (4). This feature is believed to be absolutely necessary in order to achieve high frequency broadband operation up to 11 Kmc with packaged diodes. As for lower frequency operation at 4.5 Kmc, or below, it is believed at this time that the pill diode or a slightly modified form will be adequate.

(3-b) INTEGRATED DIODES

In order to achieve the ultimate with respect to package parasitic reduction, an integrated* diode is now under development and preliminary results have shown its capability of operating well above X-band. However, a price is paid for this in the form of fragile construction. Methods of spring loading this form of diode have been developed and are currently being evaluated. As can be seen, this type of diode construction is by far the most desirable for absolute minimum parasitic reactance values.

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*The term integrated diode is used to describe a packageless type construction with the PN-junction exposed.

The reasons for acquisition of low parasitic reactances will be explained later in the section covering low pass filter limiter designs. At this point, it will suffice to say that the larger the stray series inductive reactance, the larger the apparent diode junction capacitance. This can be seen by examination of the packaged diode equivalent circuit shown in Figure (3). Since the stray inductance, L_s, is in series with the junction capacitance, C_s, it will tend to cancel out a portion of the capacitive reactance and cause C_s to appear larger than it actually is. The expression for X_s illustrates this effect.

4. THE BASIC DIODE LIMITER

As previously mentioned, PN-junction diodes can be employed to control microwave power in the form of limiters or switches. The former is of concern here though necessary microwave circuitry for either case is identical in many respects. In order to achieve efficient limiting operation, the diode must be properly arranged in a microwave circuit when placed in shunt across a transmission line, it should appear as an open circuit at low power levels and a short circuit at high levels to achieve desired operation. The ability to accomplish this is a direct result of the large impedance change exhibited by a PN-junction when subjected to the extremes in power levels.

(4-a) THE DIODE LIMITER EQUIVALENT CIRCUIT

In Figure (5), the schematic of an ideal diode limiter for narrow frequency operation is shown. Though wide band operation is the

primary concern of this program, a discussion of this circuit can be used to secure an understanding of general microwave circuitry problems involved. Also presented in Figure (5) are a set of equations relating to parameters of the packaged diode and external tuning reactances necessary to secure efficient limiting operation. These equations reduce the overall circuit to a simple normalized shunt admittance equivalent circuit representation. Once these expressions are known, $g + jb$ and $\bar{g} + j\bar{b}$, limiter performance can be calculated by use of the loss equations tabulated in Figure (6).

Returning to Figure (5), inspection shows that two external reactances, X_E and X_o are utilized. These are required to achieve minimum loss at low power levels and highest isolation at high power levels respectively*. Appropriate circuit relationships to satisfy these conditions are also shown in Figure (5). At frequencies up through S-band, this lumped circuit approach has been found to yield excellent correlation with experimental results. In all probability, this will depart to some degree at X-band but the magnitude of discrepancy has yet to be determined. For simple coax transmission line structures, diode impedance characteristics may be determined by placing a diode in shunt with the line and measuring VSWR and insertion loss. Also variation of diode

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*The value of X_o is so chosen that it resonates with $\bar{X}_T$ as shown in the diode series representation of Figure (3) under high power. This assumes R_s has changed to $\bar{R}_s$ and $\bar{X}_s$ is equal to X_{Ls}. The value of X_E is chosen to parallel resonate with the series combination of $X_T + X_o$

capacitance, by bias application, can be used to determine the exact value of L_s. In this case, X_o and X_E are omitted and C_s is varied so that series resonance and thus maximum insertion loss is secured. From the knowledge of C_s at the proper bias point and the frequency of operation, L_s can be determined.

(4-b) DIODE LIMITER CIRCUIT LOSS EQUATIONS

The loss equations tabulated in Figure (6) can be used to predict limiter performance once appropriate normalized admittance components are known. It is worthy to note that these equations are independent of the actual microwave circuitry involved and require only the normalized shunt admittance expressions of the limiter circuit; $g + jb$ and $\bar{g} + j\bar{b}$. Therefore, they represent an exceedingly valuable tool in providing a capability to analyze performance of any limiter circuit configuration. It is, of course, assumed that the transmission line itself exhibits negligible loss at the frequency of concern. This assumption can be considered quite valid up to the maximum frequency of concern, 11 Kmc.

5. THE BROADBAND LIMITER CONCEPT

In order to achieve broadband limiting, it is difficult if not impossible to employ series resonant tuning configurations as shown in Figure (5) by the use of X_o. This approach is narrow band in nature which is not compatible with the broadband performance sought after. Therefore, it appears more logical to simply place a diode in shunt with a transmission line. However, this in itself is not sufficient

with respect to low level loss unless the value of X_T, as shown in Figure (3), is much greater than the transmission line characteristic impedance Z_o. With present day diode technology, this approach seems impractical when concerned with Z_o value in the range of 25 to 50 ohms at a frequency of 11 Kmc. Therefore, microwave structures must be utilized which will be broadband in nature and employ the diode shunting impedance, X_T, in their design.

(5-a) THE LOW PASS FILTER LIMITER

One form of circuit which lends itself to use in broadband limiter designs is the low pass filter. This circuit normally takes the form of lumped shunt capacitances and series inductances forming a cascaded series of π networks as shown in Figure (7). Theory of this type structure has been adequately covered in the literature[3] and only necessary pertinent design information will be discussed here.

As can be seen in Figure (7), the circuit lends itself to use as a broadband limiter by virtue of its employment of shunt capacitors. These could obviously be secured in the form of zero biased varactors or PIN diodes provided the proper capacitance values were observed. The required series inductances can be secured through use of short sections of high impedance transmission line having a value of at least twice Z_o.

Under low power conditions, a matched low pass filter

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[3] S. B. Cohn "Direct Coupled Resonator Filters", Proc. IRE Vol. 43, pp. 187 - 196 (Feb. 1957)

designed for a sufficiently high cutoff frequency f_c would offer little attenuation to the signal. However, under high power conditions, RF interaction with the PN-junction would cause the varactor package impedance to appear as a low value of inductive reactance. This would obviously destroy the matched properties of the low pass filter structure and cause it to provide a high degree of attenuation to the incoming signal. Therefore, limiting action would be obtained. Typical response plots of the filter limiter structure under the two extreme power levels of concern are also shown in Figure (7).

The ripple exhibited by the low level response is due to the fact that a Tchebyscheff design is employed. By use of this as opposed to a Butterworth or "maximally flat" response design, greater low loss bandwidth is achieved for equal shunting capacitance values. The price paid is ripple in the operating frequency range. However, at the higher frequencies, such as X-band, this will probably be necessary due to the low anticipated capacitance values required.

Though the general approach is straightforward, several practical difficulties will be encountered. The shunting capacitance values required consist not only of the varactor or PIN junction capacitance, C_s, but parasitic effects. Therefore, actual required values will be modified by the following:

(a) Shunt package parasitic capacitance, C_p, as shown in Figure (3).

(b) Series inductance parasitic, L_s, which will cause an apparent increase in junction capacitance.

(c) Structural discontinuity capacitance as encountered at the junction of an abrupt change in coax line impedance.

(d) The inherent finite capacitance per unit length of a coax line over the physical region occupied by a diode package.

The overall effect of all these considerations will be the need of a diode junction capacitance lower in value than that predicted by theory. This at once illustrates why minimum package parasitic values (C_p and L_s) are desirable.

Returning now to the classic low pass filter theory, the various L and C values can be computated from the following expressions.

$$L_k = \frac{Z_o g_k}{\omega_c} \tag{3}$$

$$C_k = \frac{g_k}{Z_o \omega_c} \tag{4}$$

where C_k and L_k are the required filter capacitance and inductance values.

Z_o is the input and output transmission line impedance.

ω_c is equal to $2\pi f_c$ (f_c is the design cutoff frequency of the filter.)

g_k is the appropriate constant necessary for calculation of filter capacitance and reactance values (See Table I).

In all cases, n will be odd in value and $1 \leq k \leq n$. Odd values of k will be used for determination of capacitance and even values for

TABLE OF TCHEBYSCHEFF CONSTANTS, g_k, FOR LOW PASS FILTER DESIGNS

	NO. OF FILTER ELEMENTS	g_k VALUES						
		g_1	g_2	g_3	g_4	g_5	g_6	g_7
.01 DB Band Pass Ripple	3	.63	.97	.63	--	--	--	--
	5	.756	1.31	1.58	1.31	.756	--	--
	7	.797	1.39	1.75	1.63	1.75	1.39	.797
0.1 DB Band Pass Ripple	3	1.03	1.15	1.03	--	--	--	--
	5	1.15	1.37	1.98	1.37	1.15	--	--
	7	1.18	1.42	2.10	1.57	2.10	1.42	1.18
0.2 Band Pass Ripple	3	1.23	1.15	1.23	--	--	--	--
	5	1.34	1.34	2.17	1.34	1.34	--	--
	7	1.37	1.38	2.28	1.50	2.28	1.38	1.37

required inductance calculations. Once all C values are determined, parasitic and stray capacitance effects must be taken into account in order to determine the actual junction capacitance, C_s, required. As for L values, they may be secured, as previously mentioned by use of short sections of high impedance transmission line. The actual length of line required may be secured through use of the following expression.

$$L = .085\ Z_o'\ \text{nH/in.} \qquad (5)$$

where L is the inductance per unit length

Z_o' is the characteristic impedance of the high impedance line section ($Z_o' \geq Z_o$)

In practice, this method of securing an effective lumped inductance in a coaxial line structure is valid provided the line length used is less than one eighth of the filter cut-off frequency wavelength.

As a final point in this initial discussion on low pass filter limiter design techniques, a brief discussion on the isolation characteristic as a function of frequency is worth mentioning. The general isolation value trend as shown in Figure (7) shows a decreasing value as frequency increases. This is due to the fact that the diode package equivalent circuit appears as an inductive reactance when the filter limiter is subjected to high power. ($\bar{C}_s \longrightarrow \infty$). Because of this, the shorting effect of the diode becomes less effective as frequency is increased* and hence lower isolation. Here again, the desirability of low package parasitic reactance values becomes apparent.

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* As frequency increases X_{L_s} increases causing a greater deviation from a short circuit as ideally desired.

(5-b) THE BAND PASS FILTER LIMITER

For moderate bandwidth filter structures, direct coupled filters* or similar forms can be used where PN-junction diodes can provide portions of the required reactances. As an example, conventional broadband TR-tubes employ resonant iris structures of specific Q values and electrical spacings between them[4]. Normally, this spacing is a quarter wavelength at the design center frequency. However, by altering this spacing to some degree and varying the various resonant Q values[5], a considerable increase in bandwidth can be obtained. As in the previously described low pass filter case, a price is paid in the form of ripple in the low level response of the filter structure.

In the X-band region, designs have been developed at Microwave Associates for limiters exhibiting controlled low level Q characteristics which faithfully reproduce performance obtained by standard type resonant waveguide irises. To date, Q values obtainable can be made to vary from 1.0 to 10 by mechanical alteration of the waveguide limiter structure employed. Normally, the lower the Q, the lower the insertion loss and isolation. As for the latter characteristic,

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*Ibid.

[4]L. D. Smullin, C. G. Montgomery, "Microwave Duplexers", Vol. 14, Radiation Laboratory Series, McGraw Hill Book Co., 1948, pp. 76-96.

[5]L. Gould, "Filter Theory for Bandpass TR Tubes", Microwave Associates' Internal Report #4, August 8, 1957.

isolation under high power, it has the undesirable property of being frequency sensitive and exhibiting a peaked response. To a great degree, it is similar in nature to the limiter circuit previously discussed and shown in Figure (5).

In Figure (8), the general circuit employing this form of broadband limiter design is shown along with a typical response that can be expected for both insertion loss and isolation characteristics. This approach, if utilized, would be for the highest frequency range required, 7 to 11 Kmc. Moderate capacitance PN-junctions could be employed which would overcome the problem of low values needed in this range if a low pass filter design were utilized. However, here, the problem of bandwidth appears to be the most challenging.

To date, TR-tubes utilizing this technique have been designed with bandwidths up to 30%. Though this does not represent the ultimate limit, a 7 to 11 Kmc design dictates a bandwidth of 44.5% which is considerably greater. Also, broadband PN-junction limiter designs presently available at X-band are only 13% in bandwidth. Therefore, an improvement in this area by a factor of 3.4 is required.

At this early point in the program, it is anticipated that the bandpass filter technique will be used for the X-band region. This, of course, does not preclude the possibility of a waveguide low pass filter design if future work shows it to be promising.

CONCLUSIONS

At this point, with initial investigation completed, no definite conclusions based on experiment results can be made. However, the following general statements are felt to be reasonably correct on the basis of information presented in this report and past experience obtained in limiter technology at Microwave Associates.

(a) The two lower frequency ranges (1 - 4.5 and 4 - 7.5 Kmc) will, in all probability, employ some form of low pass filter limiter design.

(b) The highest frequency range (7 - 11 Kmc) seems to dictate a bandpass filter limiter design approach. However, this will depend greatly on the development of low parasistic package and integrated diodes. This is the main characteristic that precludes the employment of a low pass filter design for this case.

(c) In all cases, the employment of a PIN diode feedback limiter will be employed as the lead diode due to its inherent higher power handling capability.

PART II

PROGRAM FOR THE NEXT INTERVAL

During the next quarterly interval of this program, basic diode characteristics will be investigated with respect to the effect of package parasitics on limiting frequency of operation. This will take the form of circuit tests on existing types (pill package) and testing newer versions as they become available. In addition, filter limiter designs will be developed to cover the two lower frequency ranges of interest.

As for the X-band region, individual limiter designs will be developed and tested in an effort to extend the present capability of 13% bandwidth. As a possible alternate approach for this region, the employment of a low pass filter limiter design will be further investigated and preliminary designs developed if warranted.

Also, the area of high power diode capability investigation will be started. This will primarily involve preliminary tests and analysis on PIN feedback limiter designs over the complete frequency range of concern.

LIST OF ILLUSTRATIONS

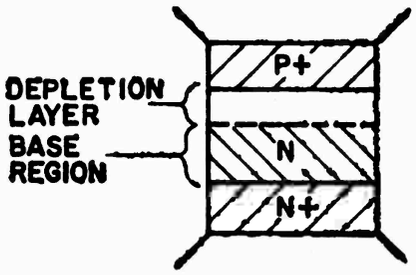
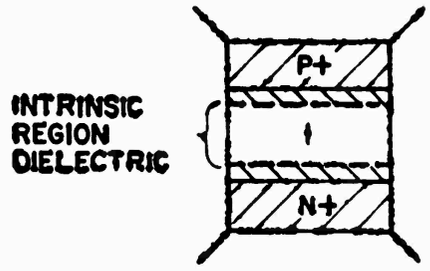
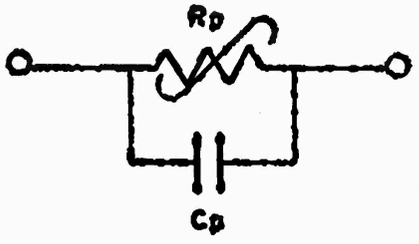
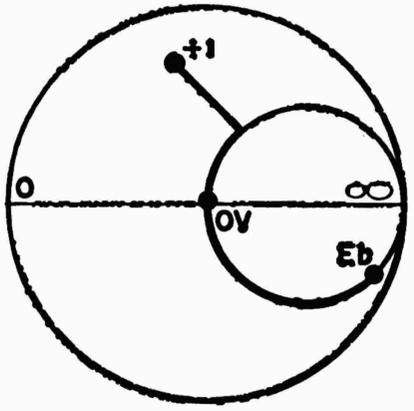
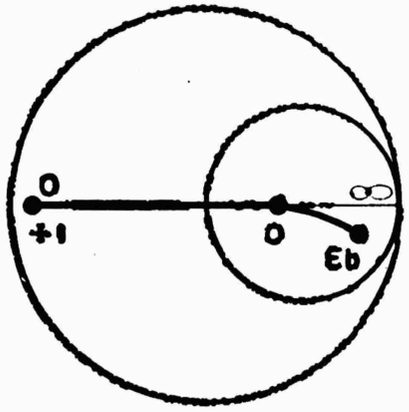
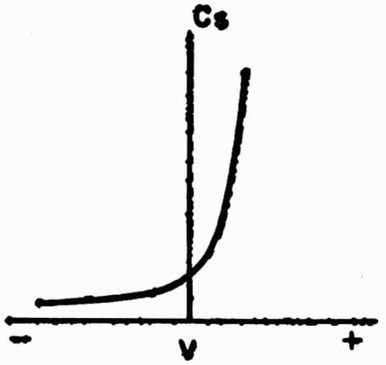
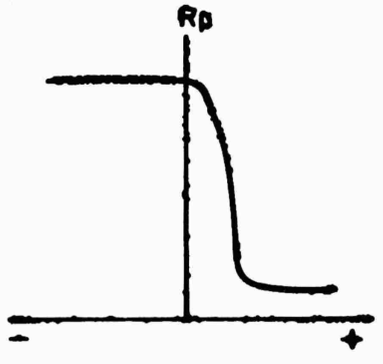
CHARACTERISTIC	VARACTOR	PIN DIODE
SCHEMATIC AT ZERO BIAS		
EQUIVALENT CIRCUIT		
TYPICAL SMITH CHART IMPEDANCE PLOT		
EQUIVALENT IMPEDANCE VOLTAGE DEPENDENT RELATIONSHIP		

FIGURE 1
GENERAL CHARACTERISTICS OF VARACTORS AND PIN DIODES

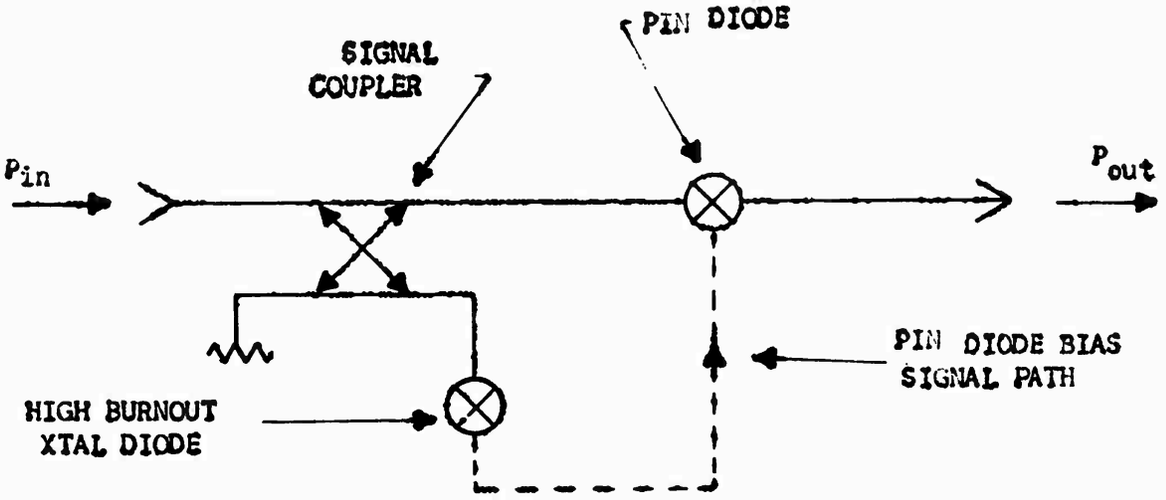
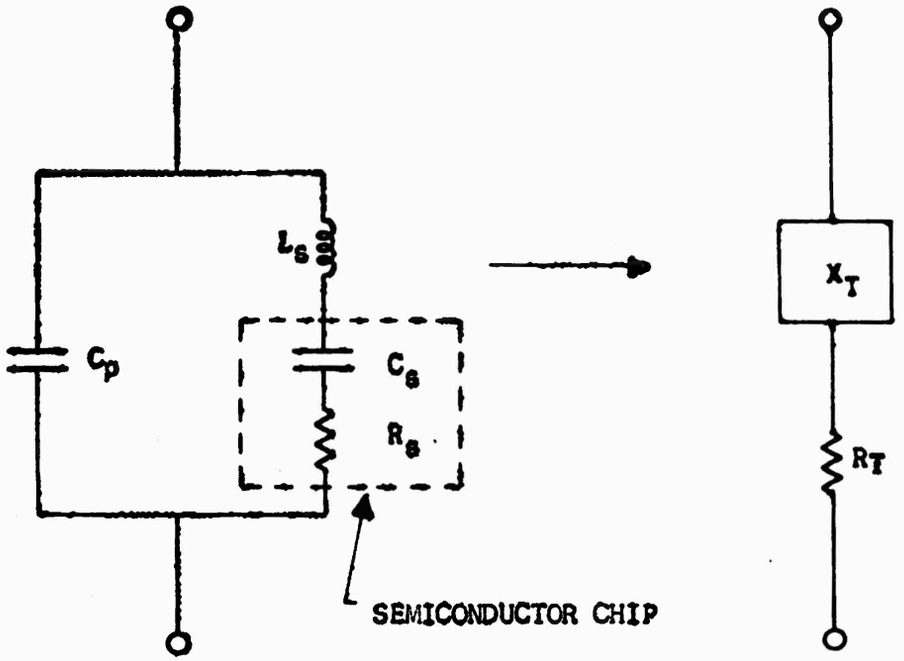


FIGURE 2

PIN DIODE FEEDBACK LIMITER CONFIGURATION
SCHEMATIC



$$R_T = \frac{X_p^2 R_s}{R_s^2 + (X_s + X_p)^2}$$

$$R_T = \frac{X_p R_s^2 + (X_s + X_p) X_s X_p}{R_s^2 + (X_s + X_p)^2}$$

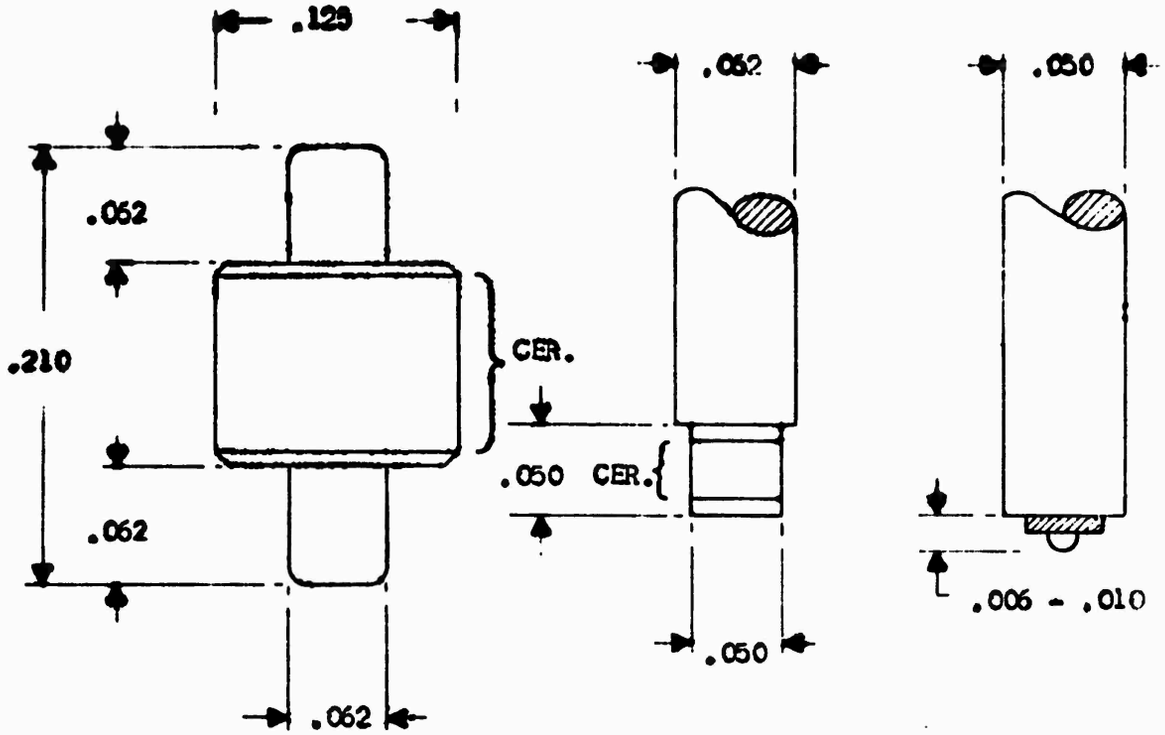
WHERE

$$X = -\frac{1}{\omega C_p}$$

$$X_s = \omega L_s - \frac{1}{\omega C_s}$$

FIGURE 3

GENERAL DIODE PACKAGE EQUIVALENT CIRCUIT AND TRANSFORMATION EQUATIONS FOR A SERIES EQUIVALENT REPRESENTATION



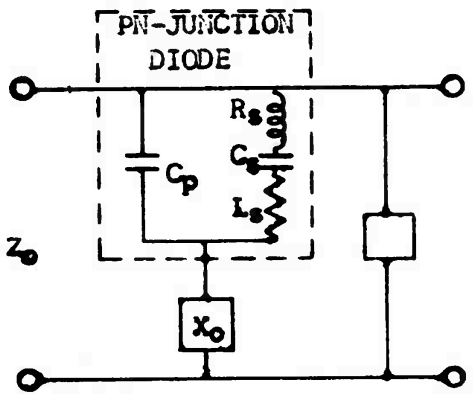
PACKAGE STYLE	L_s - SERIES INDUCTANCE	C_p- SHUNT CAPACITANCE
(a) PILL, CERAMIC	0.8 nH	0.25 pf
(b) μ - STICK, CERAMIC	0.3 nH	0.15 pf
(c) INTEGRATED	0.1 nH	NOTE 1

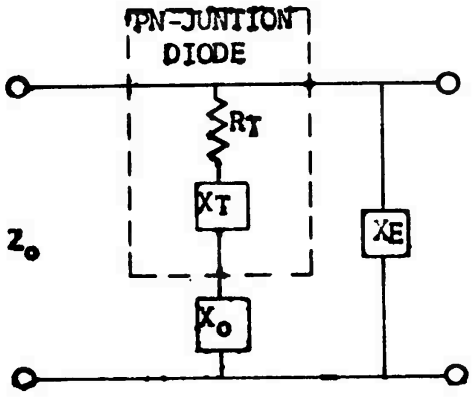
NOTES:

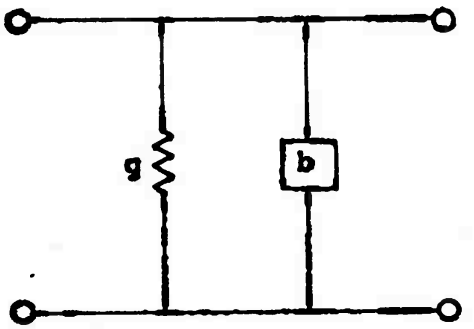
1. DEPENDENT ON MICROWAVE CIRCUITRY ENVIRONMENT, TYPICALLY < 0.1 pf

FIGURE 4

VARIOUS SWITCHING DIODE PACKAGE CONFIGURATIONS AND ASSOCIATED APPROXIMATE PARASITIC CHARACTERISTICS







ADMITTANCE COMPONENT EQUATIONS

$$g = \frac{Z_o \, R_T}{R_T^2 + (X_o + X_T)^2}$$

$$\hat{g} = \frac{Z_o \, \bar{R}_T}{\bar{R}_T^2 + (X_o + \bar{X}_T)^2}$$

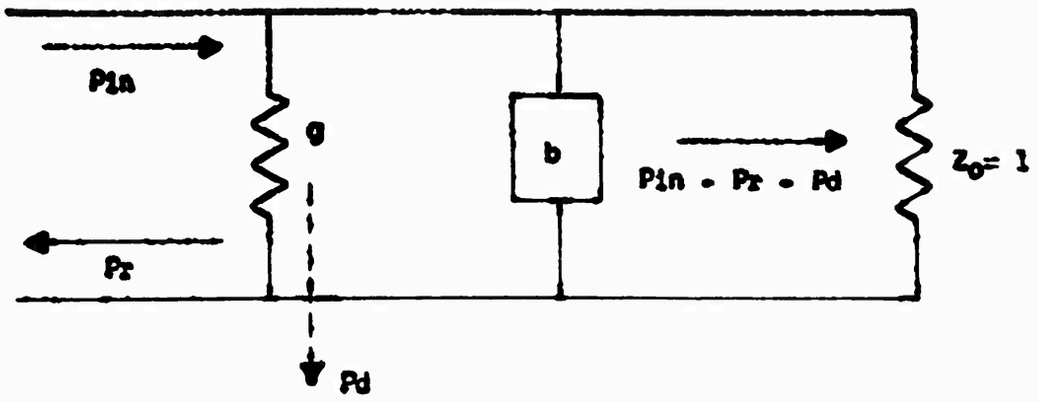
$$b = \frac{Z_o(X_o + X_T)}{R_T^2 + (X_o + X_T)^2} + \frac{Z_o}{X_E}$$

$$\hat{b} = \frac{Z_o \, (X_o + \bar{X}_T)}{\bar{R}_T^2 + (X_o + \bar{X}_T)} + \frac{Z_o}{X_E}$$

TUNING REQUIREMENTS $b=0, X_o + \bar{X}_T = 0$

FIGURE 5

PN-JUNCTION DIODE LIMITER EQUIVALENT CIRCUIT AND ASSOCIATED NORMALIZED ADMITTANCE COMPONENT EQUATIONS



$$\text{IL=INSERTION LOSS} = \frac{Pin}{Po} = \frac{Pin}{Pin-Pr-Pd} = 1 + \frac{g^2 + b^2 + 4g}{4}$$

$$\text{RL=REFLECTION LOSS} = \frac{Pin}{Pin-Pr} = 1 + \frac{g^2 + b^2}{4(1+g)}$$

$$\text{DL=DISSIPATION LOSS} = \frac{Pin}{Pin-Pd} = 1 + \frac{4g}{g^2+b^2+4}$$

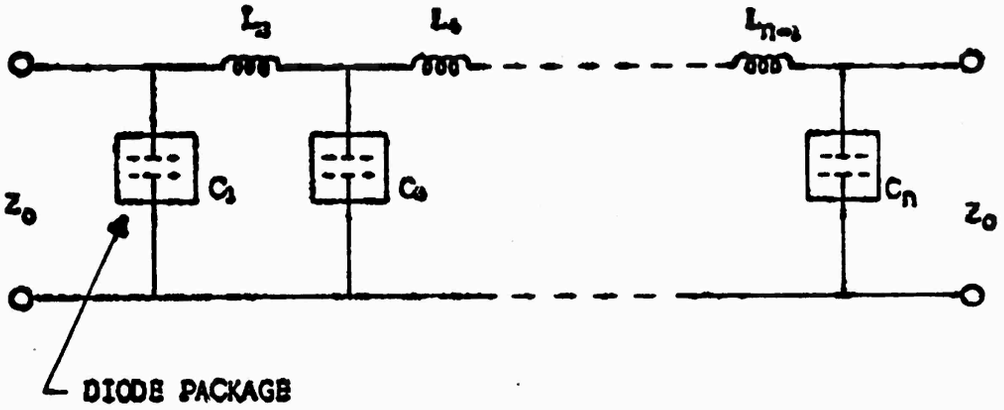
$$\%Pd = \frac{100\,(4g)}{(g+2)^2 + b^2}$$

$$\frac{1}{IL} + 1 = \frac{1}{RL} + \frac{1}{DL}$$

WHERE
- Pin IS THE INPUT POWER
- Po IS THE OUTPUT POWER
- Pr IS THE REFLECTED POWER
- Pd IS THE DISSIPATION POWER
- g IS THE NORMALIZED SHUNT CONDUCTANCE
- b IS THE NORMALIZED SHUNT SUSCEPTANCE

FIGURE 6

GENERAL SHUNT ADMITTANCE STRUCTURE LOSS EQUATIONS



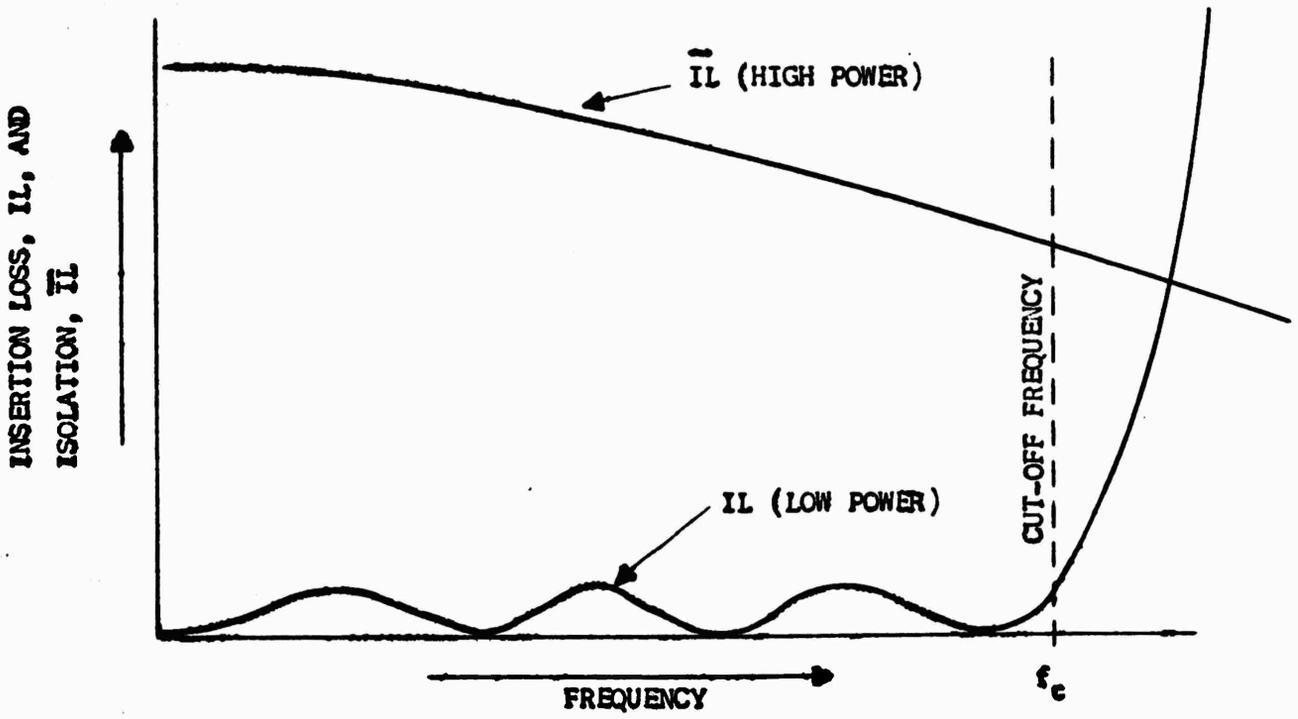


FIGURE 7

LOW PASS FILTER TYPE LIMITER EQUIVALENT CIRCUIT AND GENERAL PERFORMANCE CHARACTERISTICS

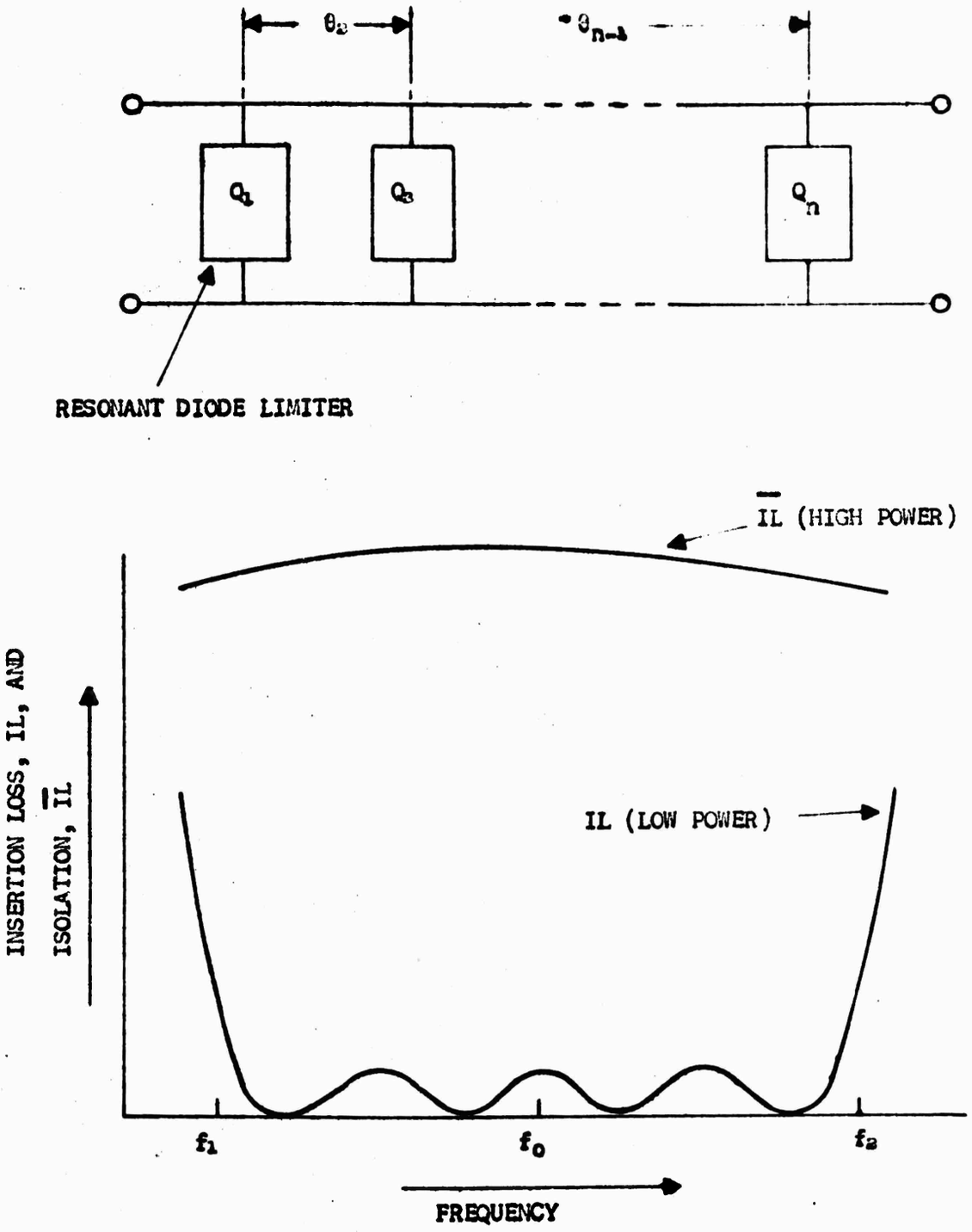


FIGURE 8

BAND PASS FILTER TYPE LIMITER EQUIVALENT CIRCUIT AND GENERAL PERFORMANCE CHARACTERISTICS